**Logo

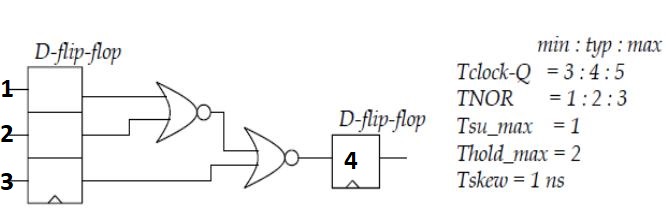
Description automatically generated San Francisco Bay University**

**EE461 Digital Design and HDL**

**Week#7 Timing Analysis in Verilog**

**IV. Exercises**

What is the fastest clock frequency given the following circuit and delay values? Is there potential for a hold violation?



Answer: To calculate the maximum clock frequency, the critical path ( longest D- flip-flop to D- flip-flop path in case of setup check) needs to be analyzed.

Based on the numbering added to the DFFs, it can be said that the longest paths are from FF1 to FF4 or from FF2 to FF4. The setup check on these paths will give the maximum operating frequency.

Applying the equation :

Tclock-Q + TNOR\_max + TNOR\_max **<** Tskew - Tsu\_max

= 5 + 3 +3 **<** 1 - 1

= 11ns

F\_max = 1 / 11 GHz

= 90.909 MHz

To check for the hold hold violation we need to consider the shortest path ( which is the critical path in this case). Here the minimum value is taken into consideration since we do not want slight changes in the flip-flop input pin while the data is being latched as it will corrupt the already present data.

the shortest path ( which is the critical path in this case) will be from ff3 to ff4 which make the hold equation to be:

TNOR\_min + Tclock-Q\_min > Thold + Tskew

= 1 + 3 > 2 + 1 or (4 > 3) which is true and hence, the circuit has no hold violation.